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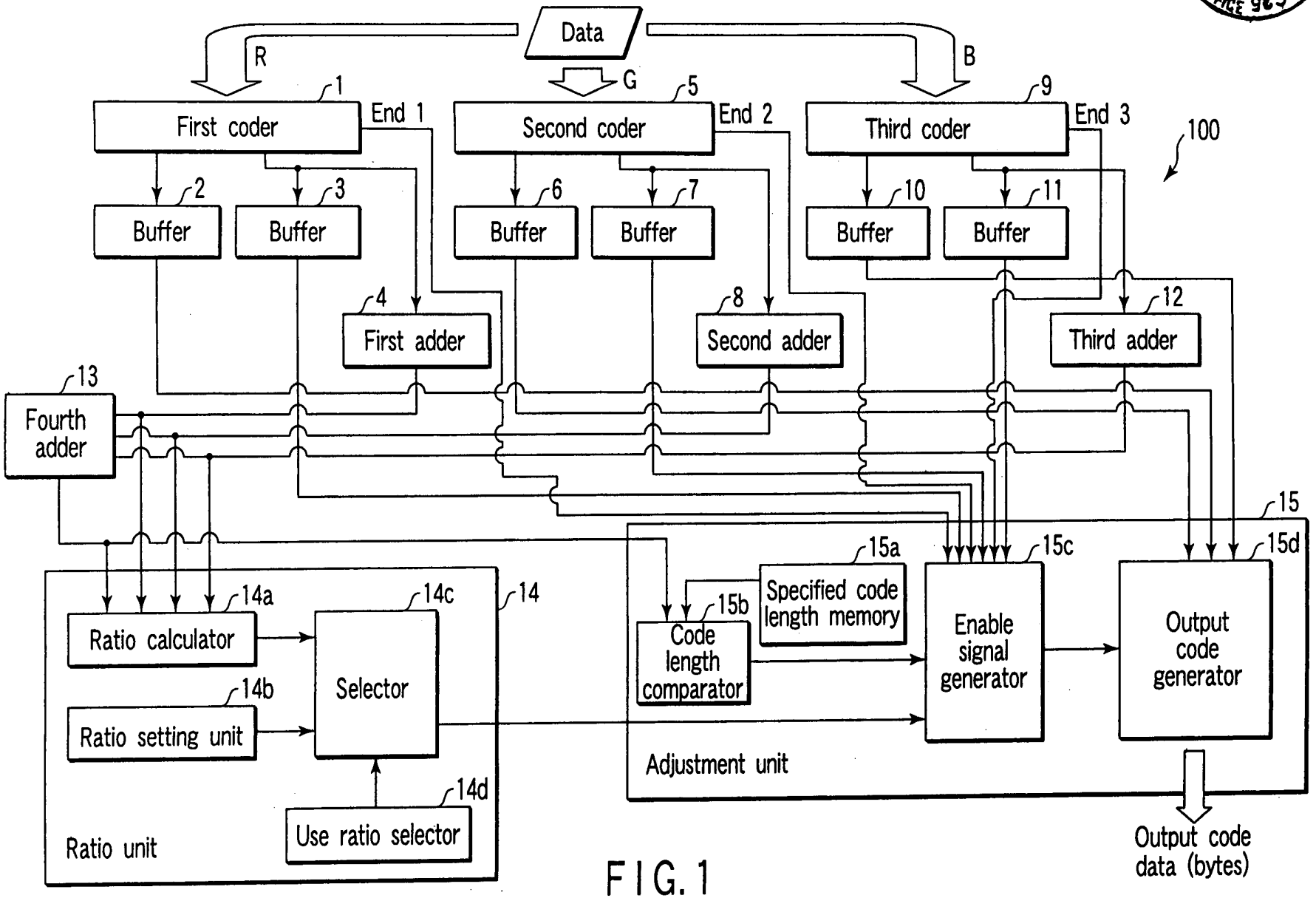

FIG. 1

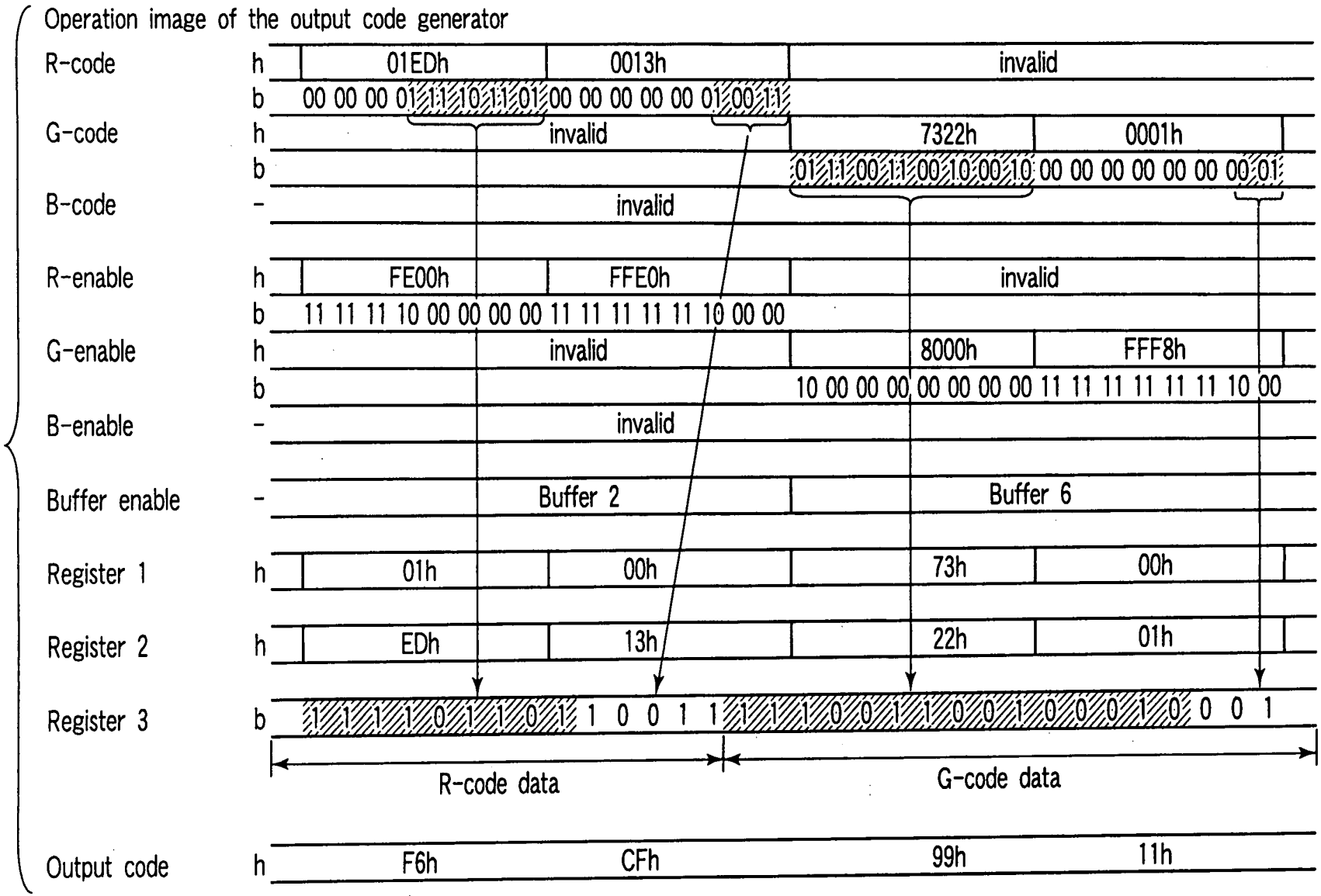
Operation image of the output code generator
R-code
G-code
B-code
R-enable
G-enable
B-enable
Buffer enable
Register 1
Register 2
Register 3
Output code
h
b
-
01EDh
0013h
invalid
00 00 00 01 11 10 11 01 00 00 00 00 00 01 00 11
7322h
0001h
01 11 00 11 00 10 00 10 00 00 00 00 00 00 00 01
FE00h
FFE0h
11 11 11 10 00 00 00 00 11 11 11 11 11 10 00 00
8000h
FFF8h
10 00 00 00 00 00 00 00 11 11 11 11 11 11 10 00
Buffer 2
Buffer 6
01h
00h
73h
00h
EDh
13h
22h
01h
1 1 1 1 0 1 1 0 1 1 0 0 1 1 1 1 1 0 0 1 1 0 0 1 0 0 0 1 0 0 0 1
R-code data
G-code data
F6h
CFh
99h
11h

FIG. 2

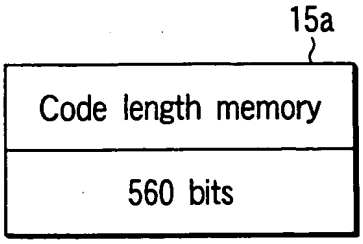

FIG. 3

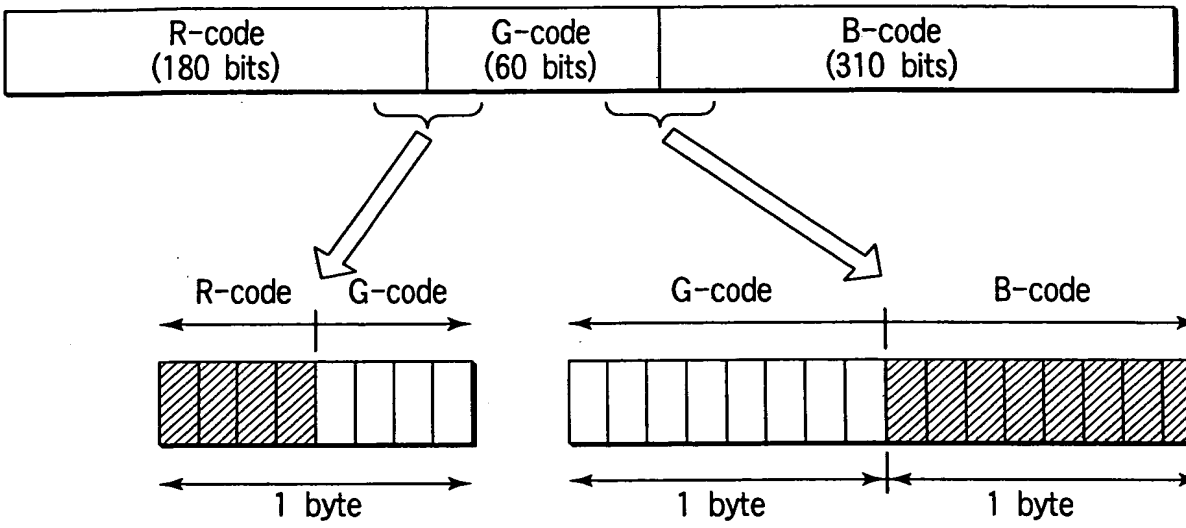

FIG. 4

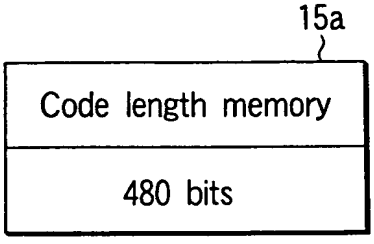

FIG. 5

	R-code (180 bits)	G-code (60 bits)	B-code (310 bits)
⋮	⋮	⋮	⋮
N-6th	7 bits	8 bits	9 bits
N-5th	4 bits	5 bits	12 bits
N-4th	6 bits	10 bits	5 bits
N-3rd	13 bits	3 bits	8 bits
N-2nd	9 bits	8 bits	4 bits
N-1st	4 bits	6 bits	8 bits
Nth	10 bits	7 bits	3 bits

FIG. 6

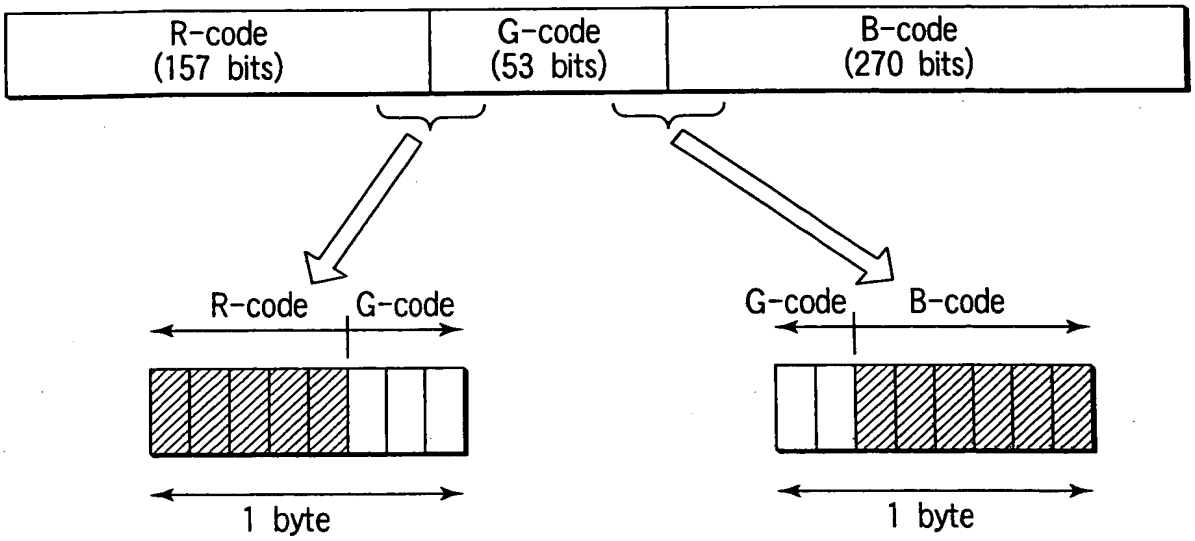

FIG. 7